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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THOMPSON, ANNETTE M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 11/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,789	CATTHOOR ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005 thru 25 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/27/05;02/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' amendment to 09/935,789, has been examined. The drawings and specification are amended. Claims 1, 7, 11-13, 15-20 are amended. Claims 1 and 3-20 are pending.

New grounds of rejection based on Applicants' IDS submission follows. The outstanding objections of the prior office action are incorporated herein.

Claim Objections

1. Claim 8 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Applicants' claim recites non-deterministic and deterministic behaviors and claims 1 and 3 do not recite any such limitation. Further it is unclear how these relations affect the steps recited by other claim limitations.

2. Claims 1 and 3-20 are objected to because of the following informalities: Pursuant to claims 12 and 20, Applicants' precatory language "is capable of" should be deleted. Pursuant to claims 1, 3, 11, 12, 13, 14, 16, 20, delete "at least" before "partly" or "in part". What is the scope of the term "at least partly". Applicants' specification gives not guidance in this regard; however one of ordinary skill in the art can fairly interpret the term "partly" or "in part" and therefore Examiner has suggested substitution of this terminology.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8, 12, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The functional relation between the "non-deterministic behavior" claim limitation and the remaining claim limitations is unclear.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Rejection of claims 1 and 3-20

5. Claims 1 and 3-20 are rejected under 35 U.S.C. 102(a) as being anticipated by the Prayati et al. paper entitled Task Concurrency Management Experiment for Power-efficient Speed-up of Embedded MPEG4 IM1 Player (hereinafter "the Prayati paper") (Publication date **August 21**-24, 2000).

6. Pursuant to claim 1, the Prayati paper discloses a method of designing a digital system, the method comprising: generating a system-level description of the functionality and timing of the digital system (§ 1, last paragraph, column 1, page 454), the system-level description comprising a plurality of tasks (Abstract); optimizing task concurrency in the system-level description to obtain a task concurrency optimized

system-level description (§ 3) that includes at least partly Pareto task optimization information (§ 5); and designing the essentially digital system based at least in part upon the task concurrency optimized system-level description (§ 5), wherein the task concurrency optimized system-level description further includes a description of a real-time operating system that uses Pareto task optimization information (Figure 3, § 5).

7. Pursuant to claim 3 the Prayati paper discloses a method of designing an essentially digital system, the method comprising generating a description of the functionality and timing of the digital system, wherein the description includes a grey-box system-level description comprising a plurality of tasks (§ 3), and wherein the grey-box system level description comprises a multi-thread graph for inter-task descriptions and a control flow graph for intra-task descriptions (§ 3, Figure 2); optimizing task concurrency in the grey-box system-level description, thereby obtaining a task concurrency optimized grey-box system level description (§ 3); and designing the essentially digital system based at least in part upon the task concurrency optimized grey-box system-level description (§ 4).

8. Pursuant to claim 4, wherein the task concurrency optimized system-level description further includes a description of a real-time operating system (Abstract and § 1, the MPEG 4 IM1 player).

9. Pursuant to claim 5, wherein optimizing task concurrency comprises separately performing design-task intra-task scheduling for at least two of the tasks, thereby generating a plurality of intra-task schedules for each of the tasks (§4).

10. Pursuant to claim 6, wherein the plurality of intra-task schedules are subset of all possible intra-task schedules, wherein the subset includes Pareto optimal schedules (§5).

11. Pursuant to claim 7, wherein optimizing task concurrently comprises designing a run-time scheduler that is part of the real-time operating system, wherein the run-time scheduler dynamically schedules at least two of the plurality of tasks (§ 7).

12. Pursuant to claim 9, wherein the digital system comprises a plurality of (§5)processors, and wherein the design –time intra-task scheduling uses processor power consumption optimization information to assign at least one of the tasks to at least one of the processors (§ 7).

13. Pursuant to claim 10, wherein at least one processor is a multi-voltage processor (§ 7).

14. Pursuant to claim 11, which recites a method of designing an essentially digital system, the method comprising generating a system-level description of the functionality and timing of the digital system (§§ 1, 3) the system-level description comprising a plurality of tasks (§ 3), optimizing task concurrency in the system-level description by separately performing design-time intra-task scheduling for at least two of the task to generate a plurality of intra-task schedules for each of the tasks (§4), wherein the plurality of intra-task schedules is a subset of all possible intra-task schedules (§5), the subset including at least partly Pareto optimal schedules (§5); obtaining a task concurrency optimized system-level description (Abstract and § 1, the MPEG 4 IM1 player)., including at least partly Pareto task optimization information, the subset

defining the Pareto task optimization information; and designing the essentially digital system based on the task concurrency optimized system-level description (§§ 3, 4).

15. Pursuant to claim 12, the Prayati paper discloses generating a system-level description of the functionality and timing of the digital system (§ 1, last paragraph, column 1, page 454), the system-level description comprising a plurality of tasks (Abstract); optimizing task concurrency in the system-level description to obtain a task concurrency optimized system-level description (§ 3) that includes at least partly Pareto task optimization information (§ 5); and designing the essentially digital system based at least in part upon the task concurrency optimized system-level description (§ 5), . . . wherein optimizing task concurrently comprises designing a run-time scheduler that is part of the real-time operating system, wherein the run-time scheduler dynamically schedules at least two of the plurality of tasks (§ 7).

16. Pursuant to claim 13, the Prayati paper discloses a program storage device tangibly embodying a program of instructions executable by the machine to perform the method (Abstract, § 1), comprising optimizing task concurrency in a system-level description of the functionality and timing of a digital system (§ 3), wherein the system-level description comprises a plurality of tasks (Abstract); wherein optimizing includes separately performing design-time intra-task scheduling for at least two of the tasks (§4), to generate a plurality of intra-task schedules for each of the tasks, wherein the plurality of intra-task schedules are a subset of all possible intra-task schedules, and wherein the subset defines at least partly Pareto task optimization information (Figure 3, § 5).

17. Pursuant to claim 14, the Prayati paper discloses a program storage device comprising selecting one or more schedules for a plurality of tasks from a plurality of at least partly Pareto optimal intra-task schedules (§5); and executing one of the tasks in accordance with the selected schedule (§ 7) .

18. Pursuant to claim 15, wherein the digital system comprises at least one processor, and wherein the design-time intra-task scheduling uses processor power consumption optimization information to determine an appropriate scheduling (§ 7).

19. Pursuant to claim 16, the Prayati paper discloses a method of designing a digital system, the method comprising: generating a system-level description of the functionality and timing of the digital system (§ 1, last paragraph, column 1, page 454), the system-level description comprising a plurality of tasks (Abstract); optimizing task concurrency in the system-level description to obtain a task concurrency optimized system-level description (§ 3) that includes cost-cycle budget tradeoff information (§ 5); and designing the essentially digital system based at least in part upon the task concurrency optimized system-level description (§ 5), wherein the task concurrency optimized system-level description further includes a description of a real-time operating system that uses the cost-cycle budget tradeoff information (Figure 3, § 5).

20. Pursuant to claim 17, the Prayati paper discloses a method of designing a digital system, the method comprising: generating a system-level description of the functionality and timing of the digital system (§ 1, last paragraph, column 1, page 454), the system-level description comprising a plurality of tasks (Abstract); optimizing task concurrency in the system-level description by separately performing design-time intra-

task scheduling for at least two of the task to generate a plurality of intra-task schedules for each of the tasks (§4), wherein the plurality of intra-task schedules is a subset of all possible intra-task schedules (§5), the subset including cost-cycle budget tradeoff information (§5); obtaining a task concurrency optimized system-level description (Abstract and § 1, the MPEG 4 IM1 player)., including cost-cycle budget tradeoff information (§5); and designing the essentially digital system based on the task concurrency optimized system-level description (§§ 3, 4).

21. Pursuant to claim 18, the Prayati paper discloses a program storage device tangibly embodying a program of instructions executable by the machine to perform the method (Abstract, § 1), comprising optimizing task concurrency in a system-level description of the functionality and timing of a digital system (§ 3), wherein the system-level description comprises a plurality of tasks (Abstract); wherein optimizing includes separately performing design-time intra-task scheduling for at least two of the tasks (§4), to generate a plurality of intra-task schedules for each of the tasks, wherein the plurality of intra-task schedules are a subset of all possible intra-task schedules, and wherein the subset defines cost-cycle budget tradeoff information (Figure 3, § 5).

22. Pursuant to claim 19, the Prayati paper discloses a program storage device tangibly embodying a program of instructions executable by the machine to perform the method (Abstract, § 1), comprising selecting one or more schedules for a plurality of tasks from a plurality of intra-task schedules based upon cost-cycle budget tradeoff information; and executing one of the tasks in accordance with the selected schedule.

23. Pursuant to claim 20, the Prayati paper discloses a method of designing an essentially digital system, the method comprising generating a description of the functionality and timing of the digital system, wherein the description includes a grey-box system-level description comprising a plurality of tasks (§ 3), optimizing task concurrency in the grey-box system-level description, to obtain a task concurrency optimized grey-box system level description (§ 3); designing the essentially digital system based at least in part upon the task concurrency optimized grey-box system-level description (§ 4); wherein . . .optimizing task concurrency comprises designing a run-time scheduler that is part of the real-time operating system, wherein the run-time scheduler dynamically schedules at least two of the plurality of tasks (§ 7).

Conclusion

24. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 27 January 2005 prompted the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

26. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(571) 273-8300, (for all OFFICIAL communications intended for entry)

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